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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/668,432	09/23/2003	Bing Lu	SC12878TP	2381

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EXAMINER	
ROSASCO, STEPHEN D	

ART UNIT	PAPER NUMBER
1756	

DATE MAILED: 11/02/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/668,432	LU ET AL.	
	Examiner	Art Unit	
	Stephen Rosasco	1756	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 October 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Detailed Action

In response to the applicant's arguments of 10/04/05 the examiner withdraws the prior office action rejection and includes a new rejection here based on newly cited art.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chiu et al. (6,777,340) in view of Chen et al. (6,887,783).

The claimed invention is directed to a bilayer hardmask used to manufacture a mask, which can be implemented to pattern a resist on a semiconductor wafer. The bilayer hardmask can have two layers: a first hardmask layer 28 and a second hardmask layer 30. The first hardmask layer 28 may be carbon and can be etched selective to the overlying second hardmask layer 30 and an underlying absorber structure 20. In another embodiment, the second hardmask layer 30 is a transparent layer of SiON, SiN, or SiOsub2. The bilayer hardmask allows for a thinner resist to be used during fabrication of the mask.

The bilayer hardmask 26 is formed over the absorber structure 20 and includes a first hardmask layer 28 and a second hardmask layer 30. The first hardmask layer 28 may be a sacrificial layer of carbon. Carbon has a high

selectivity to the desired materials of SiON and SiN for the second hardmask layer 30 and the tantalum-containing materials used for second absorber layer 24. Furthermore, carbon is desirable because it is easy to remove after the (sacrificial) layer is no longer need by exposing the carbon to an oxygen (O.sub.2) plasma. In one embodiment, the first hardmask layer 28 is approximately 70 to 100 nanometers of carbon, or more preferably is approximately 80 nanometers of carbon. The first hardmask layer 28 may be formed by physical vapor deposition (PVD), such as sputtering, PECVD, the like or combinations of the above.

Chiu et al. teach a method of using a mask in a method of patterning a silicon based layer for semiconductor devices having ultra-small devices feature size by applying an etch process, comprising the steps of: providing a silicon based layer; depositing a first layer of hard mask material over said silicon based layer; depositing a second layer of hard mask material over said first layer of hard mask material; depositing a layer of Anti Reflective Coating (ARC) material over the second hard mask layer; coating an ultra-thin layer of photoresist over the layer of ARC material; patterning and developing the ultra-thin layer of photoresist, creating a photoresist mask having a pattern of openings that aligns with a pattern of openings that are to be created in the underlying silicon based layer, said patterning and developing comprising methods of photolithography, E-beam lithography and X-ray lithography, thereby preventing tilting of the patterned layer of ultra-thin photoresist which is further enhanced by the ultra-thin nature of the

layer of photoresist; etching the layer of ARC in accordance with the pattern of openings created in the layer of photoresist; etching the second hard mask layer in accordance with the pattern of openings created in the layer of photoresist; removing the layer of developed photoresist and the etched layer of ARC from the first hard mask layer; etching the first hard mask layer in accordance with the pattern of openings created in the second hard mask layer; and etching the silicon based layer in accordance with the openings that have been etched through the first layer of hard mask material, thereby creating a pattern in said silicon based layer for semiconductor devices having ultra-small devices feature size of 0.07 mum or less.

And wherein said first hard mask layer is a silicon nitride layer with an underlying layer of silicon dioxide.

And wherein the second hard mask layer is silicon dioxide or amorphous silicon.

The teachings of Chiu et al. differ from those of the applicant in that the applicant teaches (claims 1, 8 and 15) that the first hardmask layer comprises carbon.

Chen et al. teach (see claims) a method for forming an interconnect structure on a substrate, the method comprising the steps of: depositing a dielectric material on the substrate, thereby forming a dielectric layer, depositing a hardmask material on said dielectric layer, thereby forming a hardmask layer, said hardmask layer

having a top surface; forming at least one opening in said dielectric layer; filling said opening with a conductive material, thereby forming at least one conductor, said conductor having a surface coplanar with the top surface of said hardmask layer; depositing a first material on said conductor, thereby forming a first cap layer, wherein said first material is deposited by a high density plasma chemical vapor deposition (HDP CVD) process; and depositing a second material on said first cap layer, thereby forming a second cap layer, wherein said second material is deposited by a plasma-enhanced chemical vapor deposition (PE CVD) process.

Chen et al. also teach (see col. 6, lines 8-24)

Hardmask layers 113 and 120 may be formed of any suitable dielectric material. In one preferred embodiment, hardmask layers 113 and 120 are formed of silicon nitride, and preferably have a composition of about 30 to 45 atomic % silicon, about 30 to 55 atomic % nitrogen, and about 10 to 25 atomic % hydrogen. Most preferably, these silicon nitride hardmask layers have a composition of about 41 atomic % silicon, about 41 atomic % nitrogen, and about 17.5 atomic % hydrogen. Alternatively, in another preferred embodiment, hardmask layers 113 and 120 are formed of silicon carbide, and preferably have a composition of about 20 to 40 atomic % silicon, about 20 to 50 atomic % carbon and about 20 to 45 atomic % hydrogen. A particularly preferred composition is about 27 atomic % silicon, about 36 atomic % carbon and about 37 atomic % hydrogen.

It would have been obvious to one having ordinary skill in the art to take the teachings of Chiu et al. and combine them with the teachings of Chen et al. in order to make the claimed invention because photoresist, which comprises carbon, is used to pattern the layers and is readily removed.

Applicant's arguments with respect to claims 1-20 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the Examiner should be directed to Stephen Rosasco whose telephone number is (571) 272-1389. The Examiner can normally be reached Monday-Friday, from 8:00 AM to 4:30 PM. The Examiner's supervisor, Mark Huff, can be reached on (571) 272-1385. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

S. Rosasco
Primary Examiner
Art Unit 1756

S.Rosasco
10/25/05